

FIG. 1A

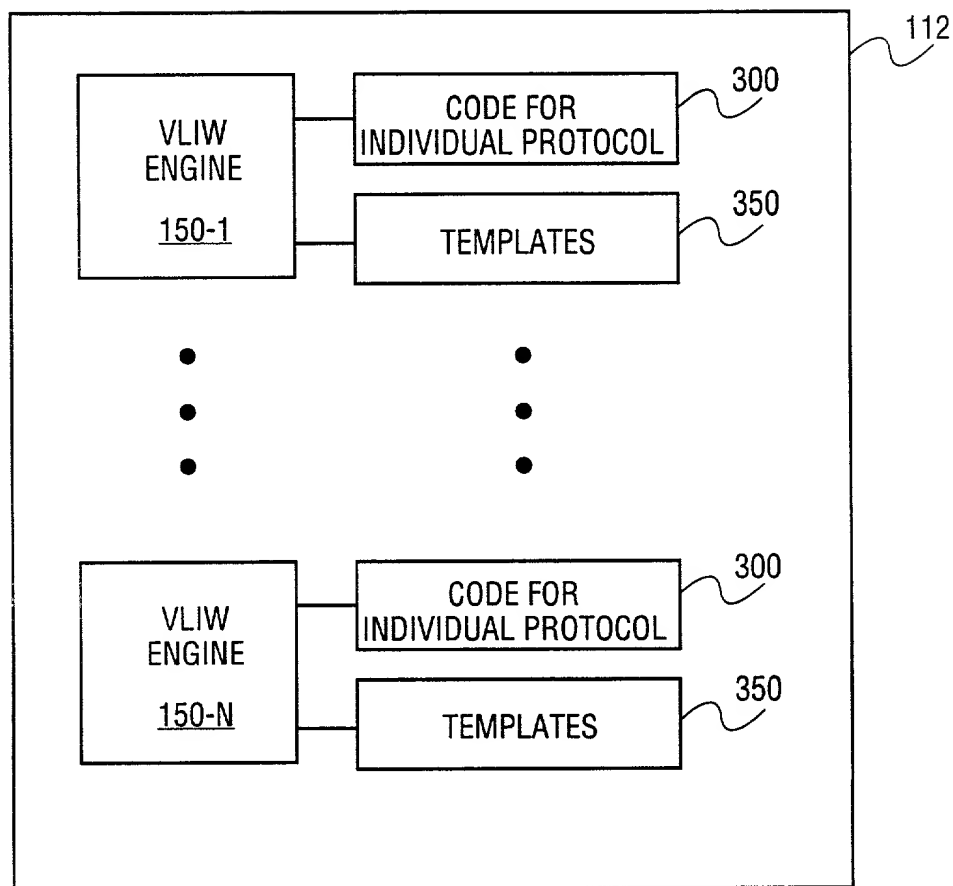


FIG. 1B

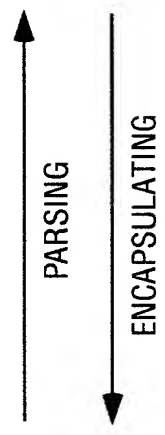
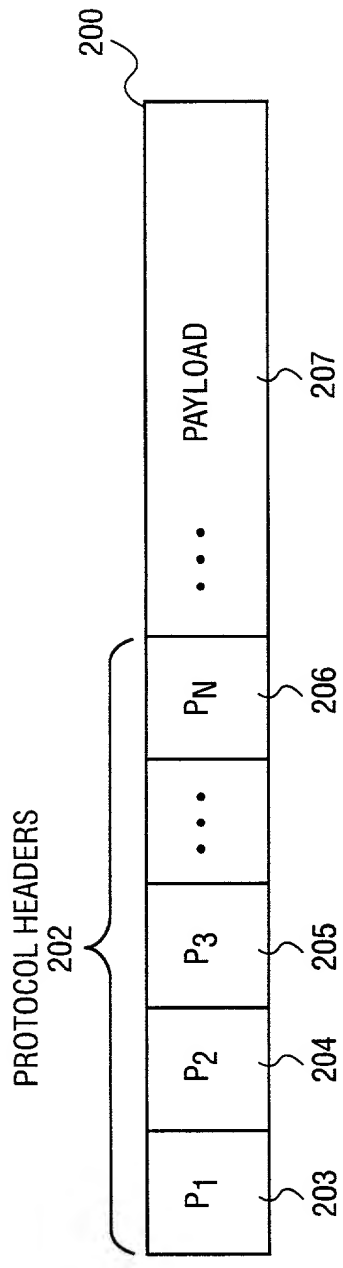


FIG. 2

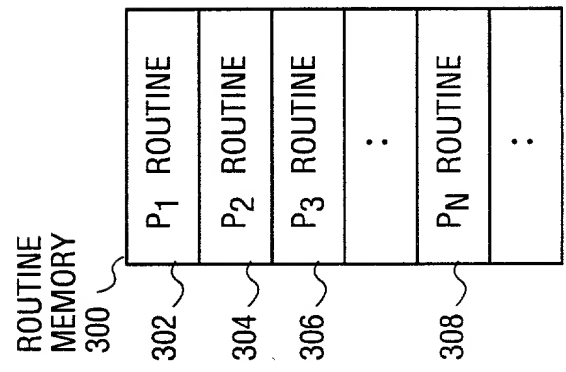


FIG. 3A

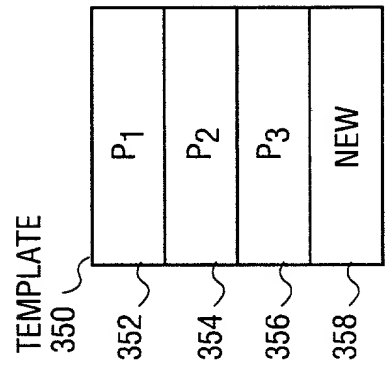


FIG. 3B

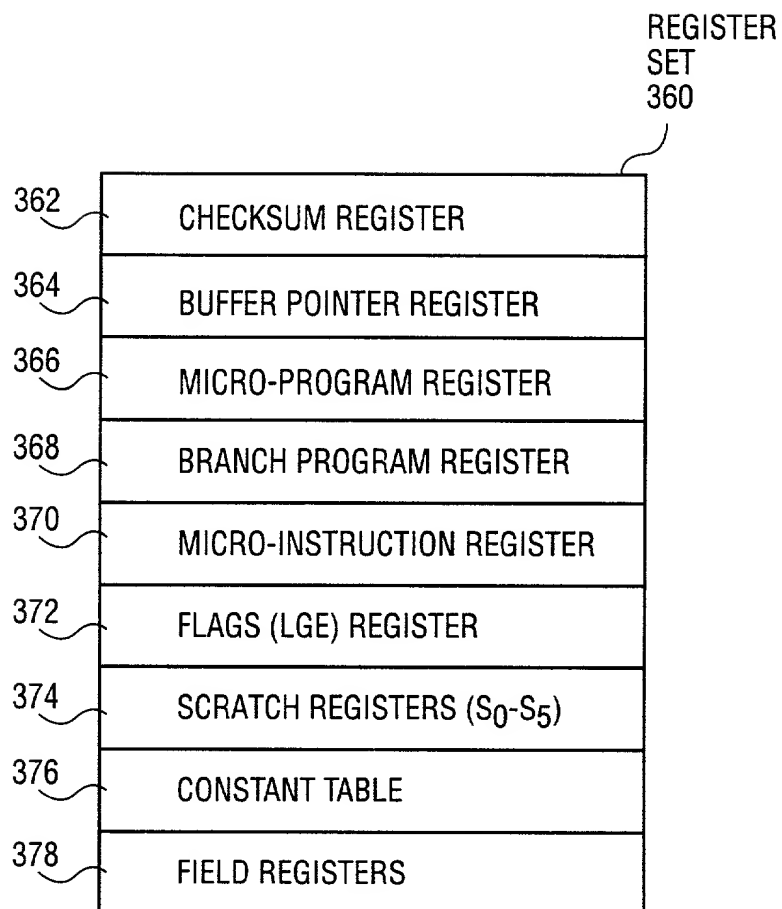


FIG. 3C

FIG. 4 is a block diagram of a system 400, according to one embodiment of the present invention. The system 400 includes a memory 402, a controller 404, a transceiver 406, a processor 408, a network interface 410, and a display 412.

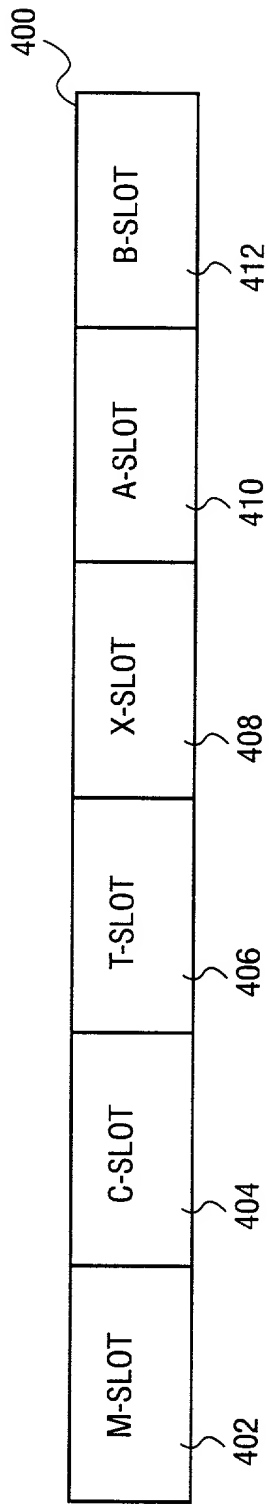


FIG. 4

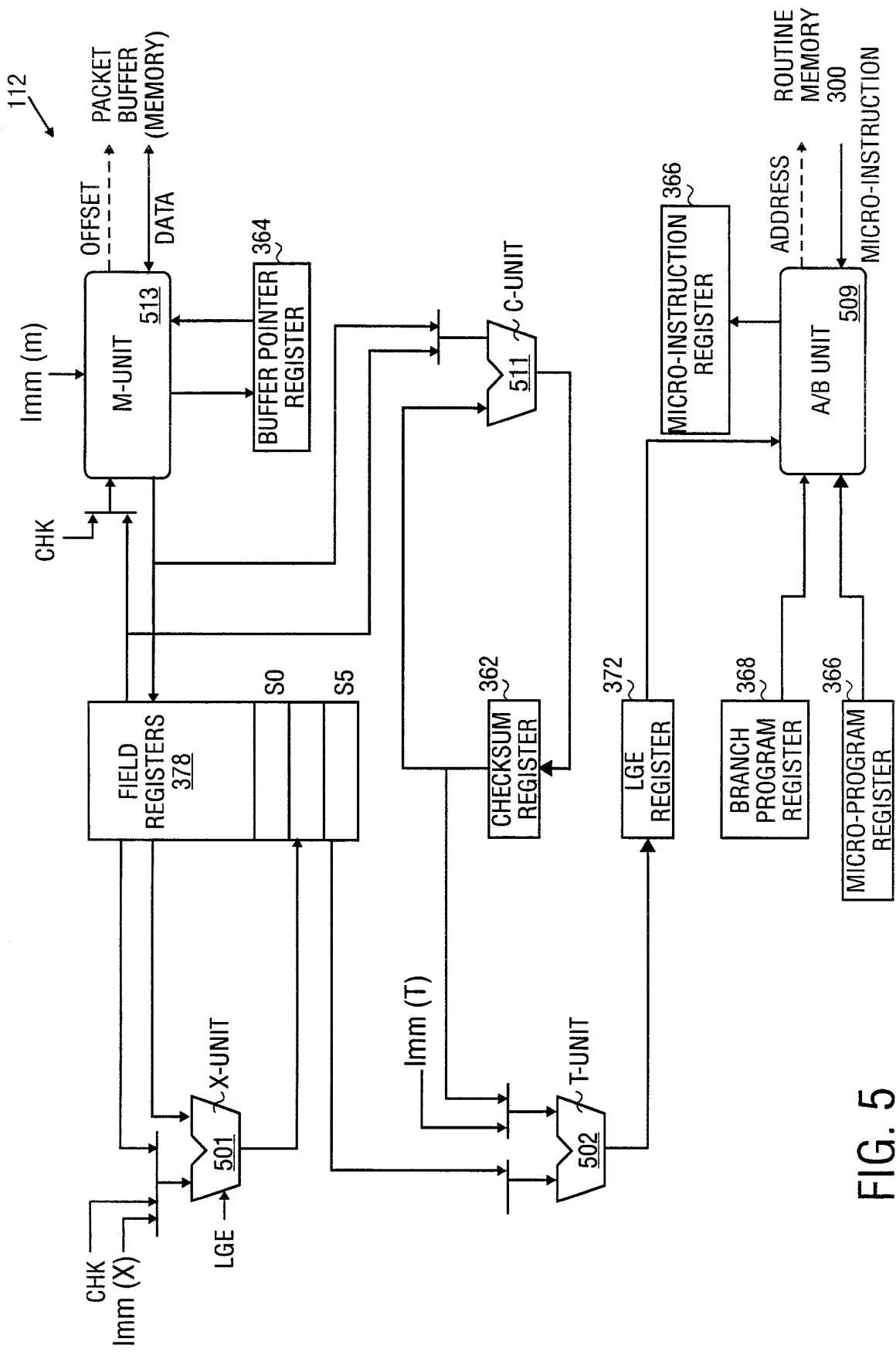


FIG. 5

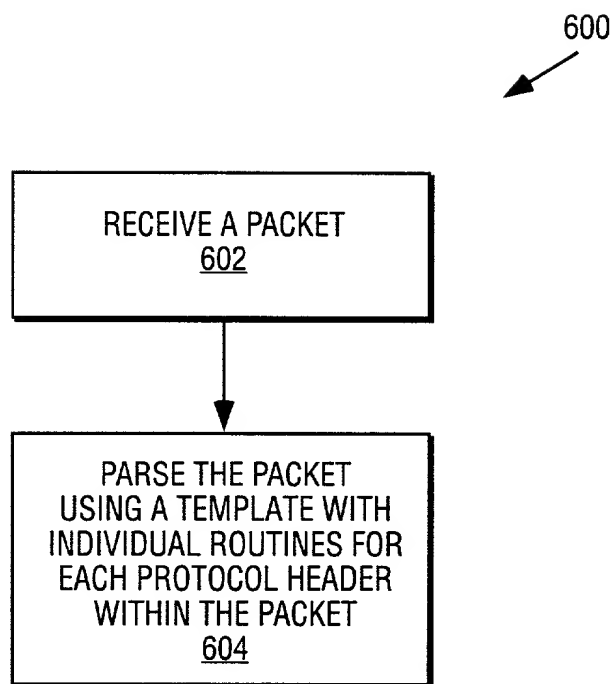


FIG. 6

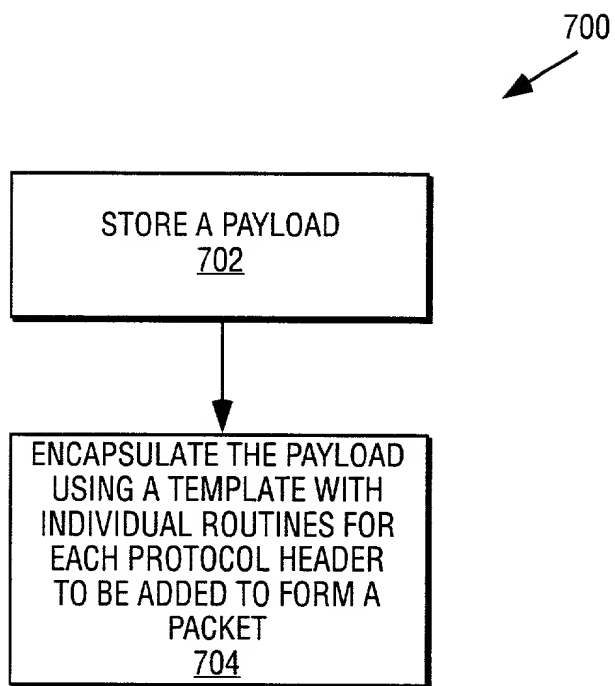


FIG. 7



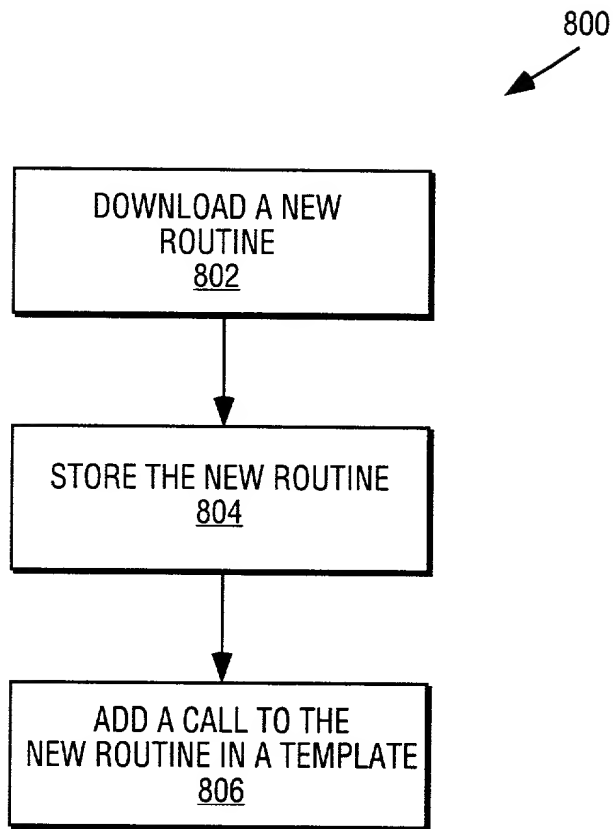


FIG. 8